PAPER

VLSI Architecture for the Low-Computation Cycle and Power-Efficient Recursive DFT/IDFT Design*

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SUMMARY   In this paper, we propose one low-computation cycle and power-efficient recursive discrete Fourier transform (DFT)/inverse DFT (IDFT) architecture adopting a hybrid of input strength reduction, the Chebyshev polynomial, and register-splitting schemes. Comparing with the existing recursive DFT/IDFT architectures, the proposed recursive architecture achieves a reduction in computation-cycle by half. Appling this novel low-computation cycle architecture, we could double the throughput rate and the channel density without increasing the operating frequency for the dual tone multi-frequency (DTMF) detector in the high channel density voice over packet (VoP) application. From the chip implementation results, the proposed architecture is capable of processing over 128 channels and each channel consumes $9.77\,\mu$W under 1.2 V @ 20 MHz in TSMC 0.13 1P8M CMOS process. The proposed VLSI implementation shows the power-efficient advantage by the low-computation cycle architecture.
key words: channel density, high density voice over packet, high throughput, low-computation cycle, power efficiency, recursive DFT/IDFT

1.   Introduction

The discrete Fourier transform (DFT) and its inverse (IDFT) are essential in the field of digital signal processing (DSP) and communication systems [14]. In the realistic world, many applications require spectrum analysis only over a subset of the N center frequencies via the DFT computation instead of the overall results of the fast Fourier transform (FFT). An effective derivative of DFT/IDFT is the Goertzel algorithm [1], [2] which emerges better performance than the FFT algorithm when only some sparse DFT results need to be obtained by completing a single complex DFT spectral bin value for every N input time instances. The Goertzel algorithm has been widely applied to the dual tone multi-frequency (DTMF) standards [3]–[8] for voice over packet (VoP) network [9]–[11] to compute the interested spectra, the discrete multitone equalizer of multicar-

rier modulation system [12], [13], and speed detection. Considering the state-of-the-art applications, the high channel-density dual-tone detector [9]–[11] is demanded. Some advanced DTMF detectors for the high density VoP network application have been realized by one embedded DSP processor [4]–[6], [9]–[11]. Although, the DSP processor based design could keep the maximum flexibility, it may not meet the cost effective considerations. On the other hand, the DSP processor based design may lose the advantages of high-throughput, low power, and small area compared with the application-specific integrated circuits (ASIC) designs [14]. In [5], the DSP processor based DTMF detectors needs a large amount of memory to decode only 24 channels, which requires 800 words data memory and 1000 words program memory with 16-bit wordlength for each words. Also, it has to operate on the higher frequency of 24 MHz. For the purpose of optimizing the whole system performance and cost, much research [15]–[22] has concentrated on the dedicated core design. In [15]–[17], the recursive expressions for the DCT computation that are suitable for VLSI implementation are presented. It is worth noticing that the recursive algorithms are solely used to design recursive DCT architectures rather than the recursive DFT architectures in [15]–[17]. In the past two decades, several recursive DFT algorithms and architectures have been explored [18]–[22]. Compared with the conventional second-order recursive DFT/IDFT architecture, Van et al. [20] utilized resource-sharing and register-splitting schemes to reduce two multipliers and speedup the computation, respectively. Yang et al. [21] proposed two unified IIR filter structures to save the hardware cost for the DFT computation. Nevertheless, neither Van et al. [20] nor Yang et al. [21] improve the computation cycle. In [22], Fan et al. applied the previous proposed method to reduce the computation cycles but the performance is limited. On the other hand, Fan et al. only proposed the recursive DFT algorithm but the IDFT algorithm is not yet ready in [22]. In essence, a short description of the proposed algorithm has been presented in the associated conference [23]. In this paper, the detailed descriptions of a high-performance and power-efficient VLSI algorithm and architecture by the hybrid of input strength reduction scheme, Chebyshev polynomial, and register-splitting scheme for the DTMF application have been fully provided. The derived algorithm and devised architecture [23] possesses the following features: low-computation cycle (i.e., high throughput) and power efficiency at the expense of slightly increased area overhead compared with the existing recursive DFT/IDFT structures.

Based on the proposed architecture, one high-throughput (i.e. high channel density) and power-efficient DTMF detector has been proposed. For the purpose of achieving the high power efficiency, we perform the bit level SNR simulation to decide the best configuration for the DTMF detector system. The results show that the proposed design only needs 9-bit word-length, which is one-bit less than the second order Goertzel structure, to land the satisfactory resolution under 15 dB SNR environment. In this paper, the resulting DTMF detector uses 12-bit word-length, where the additional 3 bits are used for design margins so as to obtain better performance. On the other hand, the novel design saves 4-bit cost compared with the 16-bit based DSP processor design [4]–[6]. In summary, the proposed DTMF structure not only saves more area cost, but also reduces the power consumption due to the register-splitting scheme [20] and a smaller word-length requirement. Most importantly, the computation cycles can be reduced to 50% and thus a double throughput rate and channel density can be easily obtained without increasing the operation frequency. Our proposed DFT/IDFT chip is able to offer over 128-channel telephone signals for the high channel density DTMF detector [8] without any DSP processor inside. Each channel consumes 9.77 μW under 1.2 V @ 20 MHz in TSMC 0.13 1P8M CMOS process. This is a significant contribution, as the high channel density and low power characteristics are demanded for the communication systems. The paper is organized as follows. A new recursive DFT/IDFT algorithm and architecture by the hybrid of input strength reduction, Chebyshev polynomial, and register-splitting schemes is revealed in Sect. 2. In Sect. 3, the DTMF application using this new architecture has been demonstrated. After the bit-level SNR simulation, the 212/106-point DFT/IDFT chip has been successfully implemented for the DTMF detector system. In Sect. 4, the comparison results are tabulated in terms of the amount of computation cycles for each output as well as N-point DFT/IDFT, the maximum number of the channel density, the clock period, and the number of real multipliers. At last, the concise statements conclude this paper in Sect. 5.

2. New Recursive Algorithm and Architecture for DFT/IDFT

The DFT of the N-point input $x[n]$ is defined as

$$y[k] = \sum_{n=0}^{N-1} x[n] \cdot W_N^{kn} = \sum_{n=0}^{N/2-1} x[n] \cdot W_N^{kn} + \sum_{n=N/2}^{N-1} x[n] \cdot W_N^{kn}, \quad (1)$$

where $W_N = e^{-j2\pi/N}$. By reducing the input strength of the DFT algorithm, Eq. (1) can be folded as

$$y[k] = \sum_{n=0}^{N/2-1} x'[n] \cdot W_N^{kn} + \sum_{n=0}^{N/2-1} x'[N-1-n] \cdot W_N^{k(N-1-n)}$$

$$= \sum_{n=0}^{N/2-1} \left(x'[n] + W_N^{-k} \cdot x'[N-1-n] \right) \cdot \cos\left(\frac{2\pi kn}{N}\right)$$

$$+ j \sum_{n=0}^{N/2-1} \left(-x'[n] + W_N^{-k} \cdot x'[N-1-n] \right) \cdot \sin\left(\frac{2\pi kn}{N}\right), \quad (2)$$

where $x'[n] = \begin{cases} x[n], & 0 \le n \le N/2 - 1 \\ 0, & \text{otherwise} \end{cases}$. Since using the input strength reduction scheme in (2), only half summation terms are needed to express $y[k]$. Equation (2) can be treated as DCT and DST parts, $y_{DCT}[k]$ and $y_{DST}[k]$, respectively, as

$$y_{DCT}[k] = \sum_{n=0}^{N/2-1} \left(x'[n] + W_N^{-k} \cdot x'[N-1-n] \right) \cdot \cos\left(\frac{2\pi kn}{N}\right), \quad (3)$$

and

$$y_{DST}[k] = -\sum_{n=0}^{N/2-1} \left(x'[n] - W_N^{-k} \cdot x'[N-1-n] \right) \cdot \sin\left(\frac{2\pi kn}{N}\right). \quad (4)$$

In (3), we can define $r_k[n] = x'[n] + W_N^{-k} \cdot x'[N-1-n]$. Replacing n by $N/2 - 1 - n$, Eq. (3) can be rewritten as

$$y_{DCT}[k] = \sum_{n=0}^{N/2-1} r_k[n] \cdot \cos\left(\frac{2\pi kn}{N}\right)$$

$$= \sum_{n=0}^{N/2-1} r_k[N/2-1-n] \cdot \cos\left(\frac{2\pi k(N/2-1-n)}{N}\right)$$

$$= (-1)^k \sum_{n=0}^{N/2-1} r_k[N/2-1-n] \cdot \cos\left(\frac{2\pi k(n+1)}{N}\right)$$

$$= (-1)^k \cdot g_{N/2-1}(k), \quad (5)$$

where $g_{N/2-1}(k) = \sum_{n=0}^{N/2-1} r_k[N/2-1-n] \cdot \cos(\frac{2\pi k(n+1)}{N})$. Let $\theta_k = \frac{2\pi k}{N}$, and $g_{N/2-1}(k)$ can be generalized as

$$g_i(k) = \sum_{n=0}^{i} r_k[i-n] \cdot \cos\left((n+1)\theta_k\right), \quad \text{where } i = N/2-1 \quad (6)$$

It is known that Chebyshev polynomials are well defined as

$$\cos(r\theta) = 2\cos((r-1)\theta) \cdot \cos\theta - \cos((r-2)\theta), \quad (7)$$

$$\sin(r\theta) = 2\sin((r-1)\theta) \cdot \cos\theta - \sin((r-2)\theta). \quad (8)$$

Using the recursive identity stated in (7), Eq. (6) can be deduced as

$$g_i(k) = \sum_{n=0}^{i} r_k[i-n] \cdot \cos\left((n+1)\theta_k\right)$$

$$= \sum_{n=0}^{i} r_k[i-n] \cdot \{2\cos(n\theta_k) \cdot \cos\theta_k - \cos((n-1)\theta_k)\}$$

$$= 2 \sum_{n=0}^{i} r_k[i-n] \cdot \cos(n\theta_k) \cdot \cos\theta_k$$

$$- \sum_{n=0}^{i} r_k[i-n] \cdot \cos((n-1)\theta_k)$$

$$= 2r_k[i] \cdot \cos\theta_k + 2 \sum_{n=0}^{i-1} r_k[i-1-n] \cdot \cos((n+1)\theta_k) \cdot \cos\theta_k$$

$$- r_k[i] \cdot \cos\theta_k - r_k[i-1]$$

$$- \sum_{n=0}^{i-2} r_k[i-2-n] \cdot \cos((n+1)\theta_k)$$

$$= r_k[i] \cdot \cos\theta_k - r_k[i-1] + 2\cos\theta_k \cdot g_{i-1}(k) - g_{i-2}(k). \quad (9)$$

The z-transform of (9) can be denoted as

$$\frac{g(k,z)}{r_k(z)} = \frac{\cos\theta_k - z^{-1}}{1 - 2\cos\theta_k z^{-1} + z^{-2}}. \quad (10)$$

For the DST part in (4), by letting $s_k[n] = x'[n] - W_N^{-k} \cdot x'[N-1-n]$ and replacing n by $N/2 - 1 - n$, $y_{DST}[k]$ can be derived as

$$y_{DST}[k] = - \sum_{n=0}^{N/2-1} s_k[n] \cdot \sin\left(\frac{2\pi kn}{N}\right)$$

$$= (-1)^k \cdot h_{N/2-1}(k), \quad (11)$$

where $h_{N/2-1}(k) = \sum_{n=0}^{N/2-1} s_k[N/2-1-n] \cdot \sin((n+1)\theta_k)$. Applying recursive identity of (8), $h_{N/2-1}(k)$ can be generalized as

$$h_j(k) = \sum_{n=0}^{j} s_k[j-n] \cdot \sin((n+1)\theta_k)$$

$$= 2 \sum_{n=0}^{j-1} s_k[j-1-n] \cdot \sin((n+1)\theta_k) \cdot \cos\theta_k$$

$$+ s_k[j] \cdot \sin\theta_k - \sum_{n=0}^{j-2} s_k[j-2-n] \cdot \sin((n+1)\theta_k)$$

$$= s_k[j] \cdot \sin\theta_k + 2\cos\theta_k \cdot h_{j-1}(k) - h_{j-2}(k). \quad (12)$$

The z-transform of (12) can be denoted as

$$\frac{h(k,z)}{s_k(z)} = \frac{\sin\theta_k}{1 - 2\cos\theta_k z^{-1} + z^{-2}}. \quad (13)$$

Equations (10) and (13) can be easily mapped into the recursive DFT structures as shown in Figs. 1(a) and (b), respectively. Compared with the conventional architectures [2], [20], [21], it is clear that by using the proposed DFT algorithm and architecture can reduce computations cycles by 50%. In other words, with respect to the algorithm derivation, the throughput rate can be easily doubled without increasing the operating frequency.

For the power-efficiency issue, we adopt the register-splitting scheme [20] (i.e., a type of retiming schemes) to reduce the critical path. There are two main advantages of using retiming scheme [24]: one is high speed and the other is low power. In this paper, we consider this technique for lowering the power consumption where the speed does not need to be increased. The resulting DCT part is depicted in the upper diagram of Fig. 2, where $\boxed{1 <=}$ denotes a hardwired shifter with one-bit left shift. Similarly, the DST part can be modified as the lower diagram of Fig. 2. In order to maintain the minimum clock period for the recursive DFT computation, the forward pipeline register, $\boxed{/}$, is exploited
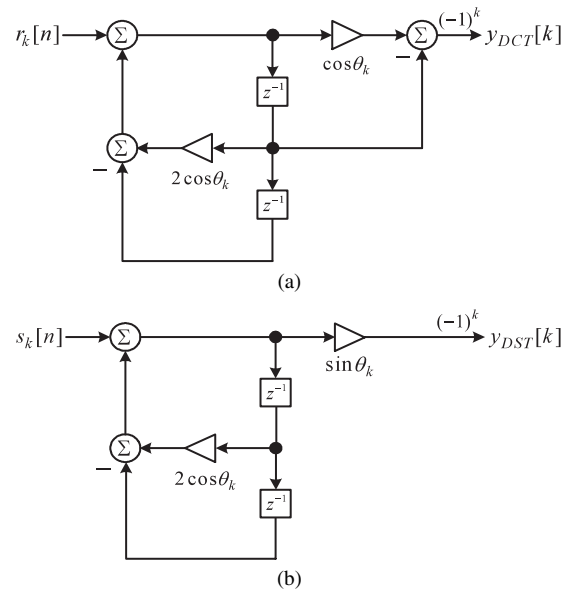

Fig. 1 Block diagram of low-computation cycle for (a) DCT part and (b) DST part of the DFT computation.
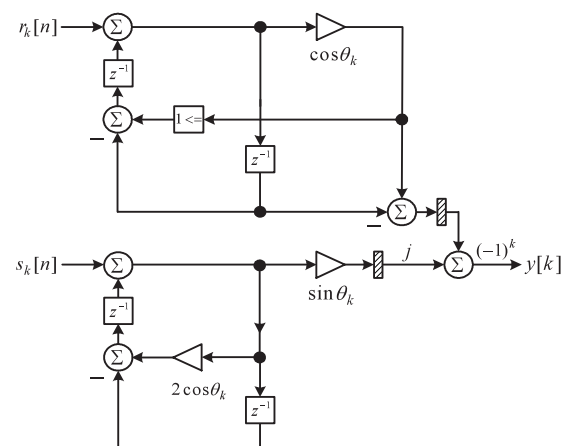

Fig. 2 Block diagram of the proposed low-computation cycle and power-efficiency recursive DFT architecture.

for the final sum output. Later combining these two new parts into one, a novel recursive DFT architecture that possesses lower computation cycle and more power-efficiency than the conventional DFT structures can be obtained.

The IDFT of the N-point input $y[k]$ is defined as

$$x[n] = \frac{1}{N} \sum_{k=0}^{N-1} y[k] \cdot W_N^{-kn}, \quad (14)$$

To develop the low-computation cycle recursive IDFT algorithm, Eq. (14) using the input strength reduction scheme can be modified as

$$x[n] = \frac{1}{N} \sum_{k=0}^{N/2-1} \left(y'[k] + W_N^n \cdot y'[N-1-k] \right) \cdot \cos\left(\frac{2\pi kn}{N}\right)$$

$$+ j \cdot \frac{1}{N} \sum_{k=0}^{N/2-1} \left(y'[k] - W_N^n \cdot y'[N-1-k] \right) \cdot \sin\left(\frac{2\pi kn}{N} \right), \quad (15)$$

where $y'[k] = \begin{cases} y[k], & 0 \leq n \leq N/2 - 1 \\ 0, & \text{otherwise} \end{cases}$. Similarly, Eq. (15) can be treated as the IDCT and IDST parts, $x_{IDCT}[n]$ and $x_{IDST}[n]$, respectively, as

$$x_{IDCT}[n] = \frac{1}{N} \sum_{k=0}^{N/2-1} \left(y'[k] + W_N^n \cdot y'[N-1-k] \right) \cdot \cos\left(\frac{2\pi kn}{N} \right),$$
$$(16)$$

$$x_{IDST}[n] = \frac{1}{N} \sum_{k=0}^{N/2-1} \left(y'[k] - W_N^n \cdot y'[N-1-k] \right) \cdot \sin\left(\frac{2\pi kn}{N} \right).$$
$$(17)$$

In (16), we can define $r_n[k] = y'[k] + W_N^n \cdot y'[N - 1 - k]$. Replacing k by $N/2-1-k$, Eq. (16) can be rewritten as

$$x_{IDCT}[n] = \frac{1}{N} \sum_{k=0}^{N/2-1} r_n[k] \cdot \cos\left(\frac{2\pi kn}{N} \right)$$
$$= \frac{(-1)^n}{N} \cdot g_{N/2-1}(n), \quad (18)$$

where

$$g_{N/2-1}(n) = \sum_{k=0}^{N/2-1} r_n[N/2 - 1 - k] \cdot \cos\left(\frac{2\pi n (k+1)}{N} \right).$$

Let $\theta_n = \frac{2\pi n}{N}$, and $g_{N/2-1}(n)$ can be generalized as

$$g_i(n) = \sum_{k=0}^{i} r_n[i - k] \cdot \cos((k + 1)\theta_n). \quad (19)$$

Using the recursive identity stated in (7), Eq. (19) can be deduced as

$$g_i(n) = \sum_{k=0}^{i} r_n[i - k] \cdot \cos((k + 1)\theta_n)$$
$$= r_n[i] \cdot \cos\theta_n - r_n[i-1] + 2\cos\theta_n \cdot g_{i-1}(n)$$
$$- g_{i-2}(n), \quad (20)$$

The z-transform of (20) can be denoted as

$$\frac{g(n,z)}{r_n(z)} = \frac{\cos\theta_n - z^{-1}}{1 - 2\cos\theta_n z^{-1} + z^{-2}}. \quad (21)$$

For the IDST part in (17), by letting $s_n[k] = y'[k] - W_N^n \cdot y'[N - 1 - k]$ and replacing k by $N/2 - 1 - k$, $x_{IDST}[n]$ can be derived in similar behavior as

$$x_{IDST}[n] = \frac{1}{N} \sum_{k=0}^{N/2-1} s_n[k] \cdot \sin\left(\frac{2\pi kn}{N} \right)$$
$$= \frac{-(-1)^n}{N} \cdot h_{N/2-1}(n), \quad (22)$$

where $h_{N/2-1}(n) = \sum_{k=0}^{N/2-1} s_n[N/2 - 1 - k] \cdot \sin((k+1)\theta_n)$.
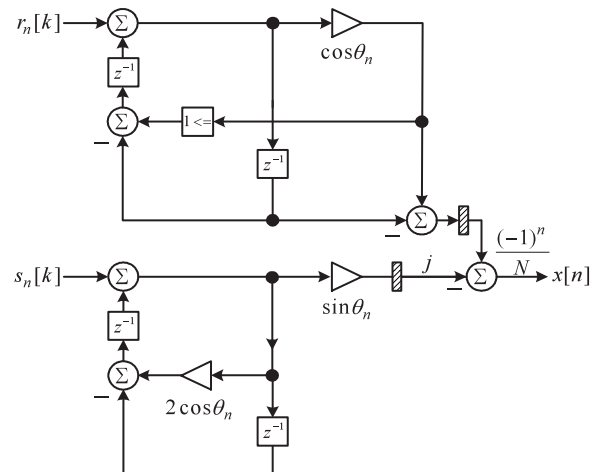

Fig. 3 Block diagram of the proposed low-computation cycle and power-efficient recursive IDFT architecture.

Applying (8), $h_{N/2-1}(n)$ can be generalized as

$$h_j(n) = \sum_{k=0}^{j} s_n[j - k] \cdot \sin((k + 1)\theta_n)$$
$$= s_n[j] \cdot \sin\theta_n + 2\cos\theta_n \cdot h_{j-1}(n) - h_{j-2}(n). \quad (23)$$

The z-transform of (23) can be denoted as

$$\frac{h(n,z)}{s_n(z)} = \frac{\sin\theta_n}{1 - 2\cos\theta_n z^{-1} + z^{-2}}. \quad (24)$$

After using the register-splitting scheme, Eqs. (21) and (24) can be easily mapped into the modified structures as shown in Fig. 3. Again, from the proposed algorithm and architecture, it is obviously found that the 50% computation cycle reduction can be achieved by contrast with that of [2], [20], [21]. That means double the throughput rate can be achieved under the same operating frequency.

3. Application and Chip Implementation

In this paper, we are encouraged to design a low-computation cycle (i.e., high throughput) and power-efficient (i.e., cost-effective) recursive DFT/IDFT architecture for the high channel density DTMF detector in the VoP application. So as to reach this purpose, we follow two down-to-earth steps to optimize our target design. First, according to the dataflow of the DTMF detection as shown in Fig. 4 [5], we could find that the DTMF detector enables one channel telephone [5] to provide 14 different recursive DFT computations. The total computations for the DTMF detector include 6 106-sample frames and 8 212-sample frames. Thus, we proposed one high channel density DTMF detector to handle both 212 and 106-sample frames based on the proposed recursive core architecture as shown in Fig. 5. The proposed architecture in the first 106-sample frame needs full 106 clock cycles because it involves extra 53 clock cycles for the input data latency. The other 5 106-sample frames only require 53×5 clock cycles, and 8 212-sample
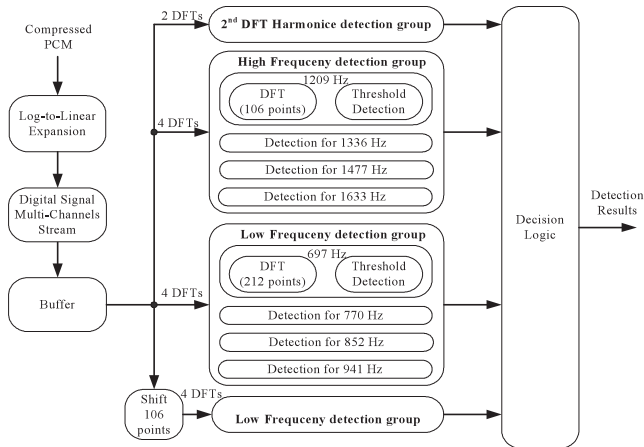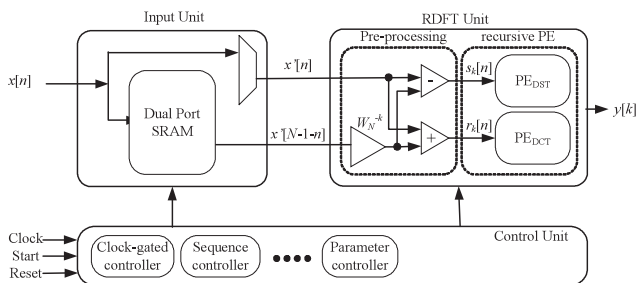
Fig. 4   Dataflow of the DTMF detection [5].

Fig. 5   Block diagram of the proposed high channel density DTMF architecture.

Fig. 6   Bit level SNR simulation environment.

Fig. 7   Bit level SNR simulation results.

frames only require 106×8 clock cycles. Besides, the RDFT unit needs 14 reset clock cycle to initialize each frame computation. In total, one channel DTMF detection process would only require 1,233 clock cycles per window. On the contrary, based on the second-order Goertzel structure, one channel DTMF detection would require 2,346 clock cycles for each window, which is almost twice the latency of the proposed framework.

The high channel density DTMF detector as depicted in Fig. 5 consists of the recursive DFT (RDFT) units, an input unit, and a control unit. The behaviors of the above units are described as follows:

RDFT Unit: The RDFT unit as depicted in Fig. 5 consists of one pre-processing element and one recursive processing element (PE). The pre-processing element is able to provide the intermediary data s_k and r_k to the following recursive PE. Recalling (5), (11), (18), and (22), our proposed VLSI algorithm only needs $N/2$ clock cycles to accomplish each output data sequence.

Input Unit: The input unit is composed of a dual port SRAM that can store 318 complex data sequences. It could serve two sizes of input data buffer: 106 and 212 samples. According to the proper scheduling, the input unit can provide the dual data $x'[n]$ and $x'[N-1-n]$ for the pre-processing element of the RDFT unit.

Control Unit: The control unit not only plays the role of the data sequence controller but also a parameter con-
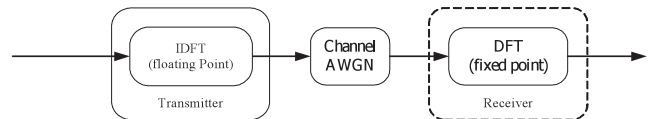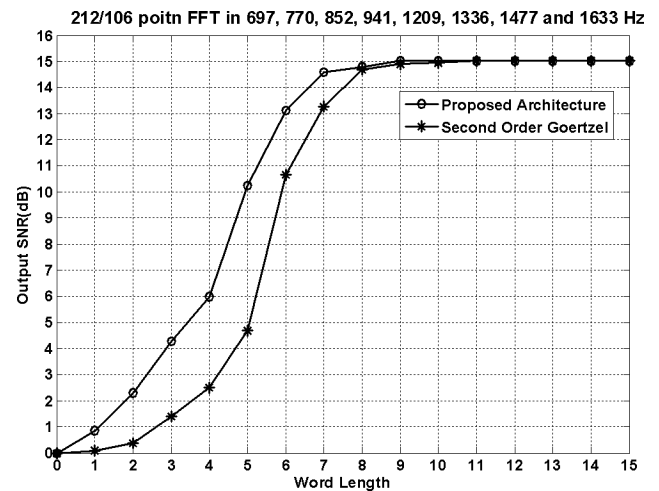
troller, which feeds the proper coefficients to the RDFT units. In this paper, since the input data and output data of the proposed architecture are all controlled in the serial manner, the desired output data can be obtained for each $N/2$ clock cycles.
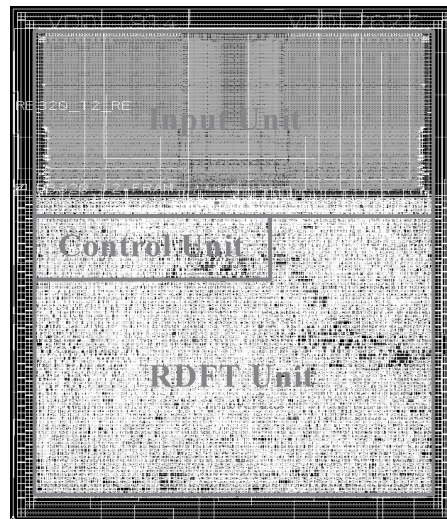
Next, we adopt the bit-level SNR simulation to estimate the appropriate word-length under the ITU specification [3] to further reduce the chip area and power consumption. We know that the DTMF detector must operate properly under 15 dB SNR or higher. Thus, we set the simulation environment as depicted in Fig. 6 under 15 dB with additive white Gaussian noise (AWGN) channel model. Then, we will only consider the DFT part in the receiver side for the DTMF detector. In Fig. 6, the input signal $x[n]$ passes thought IDFT block and then propagates through the channel, where the above operations run at floating point simulation. In the receiver side, the receiver signal is quantized into the fixed bits and performs the fixed-point DFT calculation. We perform the system simulation of 212/106-sample frames at the 8 DTMF signal frequency bins: 697, 770, 852, 941, 1209, 1336, 1477 and 1633 Hz as shown in Fig. 4. In Fig. 7, the x-axis and y-axis denote the data word-length and the whole system output SNR, respectively. We can observe that the output SNR will saturate as data word-length increases. It is manifest that the proposed recursive architecture only needs 9-bit resolution, which is less than 10-bit of the second-order Goertzel structure. That means we need less hardware resources to achieve the ITU performance requirements under our proposed architecture. In other words, if we select the same word-length for the proposed and Goertzel based designs, the former is able to offer the higher

Table 1 Chip characteristics of the proposed DTMF detector.

Maximum Channel Number	128
DFT Length (N)	212/106 points
Input Word Length (w)	12 bits
Critical Delay Time	43.12 ns
Chip Area	387 μm x 469 μm
Power Consumption per channel	9.77 μW@20 MHz
Process Technology	TSMC 0.13 μm CMOS

Fig. 8 212/106-point recursive DFT/IDFT chip layout.

design margin for better system performance. In this case, because 3-bit design margin is sufficient, we choose the data word-length as 12-bit wide.

Concerning the chip implementation, our target is 212/106-point DFT/IDFT for high channel density DTMF detector [9]–[11]. As we know, the ITU timing specification indicates that the durations of DTMF signal detection and non-detection must be at least 40 ms and less than 23 ms, respectively. At a sampling rate of 8 KHz, a 106-sample frame size corresponds to a 13.3 ms window. After each window, the detected signal is compared to the last and second-to-last values. If the result of the new window is the same as the last, but different from the second-to-last, then a new valid DTMF signal has been found [5]. Recall that the proposed architecture requires 1233 clock cycles to finish one channel DTMF detection for each window. In this paper, the operating frequency and guard time are targeted at 20 MHz and 31.6 ms, respectively. That means we only need 61.65 μs (i.e., 1233 × 50 ns) to finish one window computation for one channel DTMF detection. Accompany with the DTMF FSM controller [5], the proposed design can detect up to 128-channel DTMF signals, which is superior to [4]–[6]. The implementation processes are as follows. First, the Cadence NC-Simulator is used as the Verilog functional verification, so the outputs from the RTL model are validated against a standard LabVIEW model. Then, the 212/106-point recursive DFT/IDFT architecture in which the internal word-length is 12-bit has been synthesized with the Design Compiler in TSMC 0.13 μm CMOS technology. After the post simulation, at the present stage, the critical path is 43.12 ns in TSMC 0.13 μm CMOS process. Consequently, the proposed design is very suitable for DTMF detector system. The floorplan as well as the post-layout have been carried out using Astro. After the back-annotation from Start-RC extractor, the post-simulation has been issued by NC-Simulator to verify the functionality. The static timing check can be signed-off by PrimeTime. Finally, the power analysis and LVS can be done by Astro Rail and Dracula, respectively. For post layout, the core area is $0.18 \, mm^2$. The chip characteristics listed in Table 1 shows that the average power dissipation of the proposed high channel density DTMF detector is 1.25 mW@20 MHz at 1.2 V supply voltage. It is worth to notice that the proposed design could handle the 128 DTMF channel, that means each channel only consumes 9.77 μW after the division of 128. The micropho-

tograph of the 212/106-point recursive DFT/IDFT core design as shown in Fig. 8 has been implemented as one hard IP (Intellectual Property). In this way, the proposed architecture and chip can be reused in the system-on-a-chip (SOC) platform. The proposed 212/106-point recursive DFT/IDFT design not only meets 40 ms timing specification for ITU standard, but also achieves the low power consumption due to the register-splitting scheme and smaller bit-width requirement compared with the design of [4]–[6].

4. Comparison Discussion

In this section, we give a comprehensive comparison result as listed in Table 2 in terms of the number of computation cycles for each DFT/IDFT output as well as N-point DFT/IDFT calculation, the maximum number of channel density, the clock period, and the number of real multipliers. Note that the operation time of a complex multiplication requires $T_m + T_a$. Our proposed work [23] based on the input strength reduction scheme can save half computation cycles for each DFT/IDFT output compared with the existing works [2], [20], [21] at the expense of slightly increased area cost. Note that we make a comparison between our proposed work and the best case design of [21], FAST fixed-coefficient recursive DFT (FFR-DFT), in terms of specific terminologies in Table 2. At the same time, the reference structure of [2] is the block diagram as shown in Fig. 9.2 of [2]. Compared with the results of the recursive algorithm in [22] which, for example, requires 2794 computational cycles to obtain all 64-point DFT outputs, the proposed core-type architecture requires 2048 computational cycles. In other words, our proposed work exploiting the input strength reduction scheme has the lowest computation cycles among existing structures [2], [20]–[22]. As a consequence, our proposed architecture is capable of providing the highest channel density in the DTMF communication system. From the implementation results, it is obviously

Table 2 Comparison results among the recursive DFT/IDFT architectures.

Parameters	Second Order DFT/IDFT [2]	V-Ys' Structure [20] (Core Type)	Y-Cs' Structure [21] (FFR-DFT)	Proposed Work
# of Computation Cycles for Each $y[k]$ or $x[n]$	N	N	N	$N/2$
# of Computation Cycles for N-Point DFT/IDFT	N^2	N^2	N^2	$N^2/2$
Maximum of Channel Density (in TSMC 0.13 μm)	64	64	64	128
Clock Period	$T_m + 3T_a$	$T_m + 2T_a$	$2T_m + 5T_a$	$T_m + 2T_a$
# of Real Multipliers	6	4	6 (Pre-processing Excluded)	6 (Pre-processing Excluded)

seen that the channel amount of the proposed architecture is double compared with other designs [2], [20], [21]. Since exploiting the register-splitting scheme, the proposed one inherently has higher speed than the recursive structures of [2], [21], [22] and possesses the same operating frequency as that of our previous work [20]. According to the critical path comparison in Table 2, the proposed DFT/IDFT fabric owns $T_m + 2T_a$ clock period and the clock periods in [2], [21], [22] are of $T_m + 3T_a$, $T_m + 2T_a$, and $2T_m + 5T_a$, respectively. As mentioned in Sect. 2, the register-splitting scheme either achieves high speed or low power computation. In this article, we consider this technique for lowering the power consumption where the speed does not need to be increased [24]. In Table 2, if the architecture possesses a shorter clock period, less power consumption can be achieved while keeping the same clock rate. However, considering the hardware complexity, the proposed DFT/IDFT architecture requires two more multipliers than the previously proposed one [20]. Furthermore, based on the proposed work, we can easily construct a parallel-type recursive DFT/IDFT architecture for other applications such as the matching filter and equalizer. The parallel-type architecture can significantly reduce the number of computation cycles for N-point DFT/IDFT from $N^2/2$ to $\frac{N}{2} \cdot \left\lceil \frac{N}{P} \right\rceil$, where P is the number of RDFT and $\lceil \bullet \rceil$ indicates the minimum integer value greater than or equal to $\bullet$. Thus, the maximum throughput can be achieved. As a consequence, in Table 2, it reveals that our proposed architecture has characteristics of the lowest computation cycle (i.e., highest throughput), the maximum number of channel density, and power efficiency.

5. Conclusion

One new recursive DFT/IDFT algorithm and architecture based on a hybrid of input strength reduction scheme, the Chebyshev polynomial and register-splitting scheme is devised in this framework. The analyzed results show that the proposed VLSI algorithm leads to the fewest computation cycle and the highest throughput rate. Moreover, the proposed 212/106-point recursive DFT/IDFT chip design has been successfully implemented in 0.13 μm CMOS technology and possesses the power-efficiency consumption of 9.77 μW @ 20 MHz at 1.2 V supply voltage for each channel.

These features guarantee that the proposed high-throughput and power-efficient VLSI architecture is certainly amenable to high channel density DTMF systems.

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